LISTING OF THE CLAIMS

Please amend the Claims as follows:

1. (original) A voltage trim circuit comprising:

an operational amplifier coupled to an input node;

a transistor coupled to said operational amplifier and for receiving a first potential;

a voltage divider circuit coupled to said operational amplifier, said transistor and an output, wherein an output voltage is generated as a function of an adjustable divider ratio, and wherein a substantially constant feedback path is provided to said operational amplifier; and

a bias current circuit coupled to said voltage divider circuit and a second potential, wherein an adjustable resistive load is configurable to maintain a substantially constant load current through said transistor.

2. (original) The voltage trim circuit according to Claim 1, wherein

said input node is coupled to an inverting input of said operational amplifier;

said output of said operational amplifier is coupled to a gate of said transistor;

said first potential is coupled to a source of said transistor;

a drain of said transistor is coupled to a first terminal of said voltage divider;

a second terminal of said voltage divider circuit is coupled to a non-inverting input of said operational amplifier;

a third terminal of said voltage divider circuit is coupled to said output

a fourth terminal of said voltage divider circuit is coupled to a first terminal of said bias current circuit; and

a second terminal of said bias current circuit is coupled to said second potential.

3. (original) The voltage trim circuit according to Claim 1, wherein said voltage divider circuit comprises:

a series resistor circuit coupled between said transistor and said bias current circuit; and

a plurality of selector elements, wherein each selector element is coupled between a corresponding node of said series resistor circuit and said output.

4. (original) The voltage trim circuit according to Claim 1, wherein said bias current circuit comprises:

a series resistor circuit coupled between said voltage divider circuit and said second potential; and

a plurality of shunt elements, wherein each shunt element is coupled in parallel with a corresponding one of a first portion of resistors of said series resistor circuit.

5. (original) The voltage trim circuit according to Claim 4, wherein said first portion of said series resistor circuit comprises:

a first set of binary weighted resistors; and

a second set of binary weighted resistors.

6. (original) The voltage trim circuit according to Claim 1, wherein said substantially constant load current is adapted to reduce instability in said voltage trim circuit.

7. (original) The voltage trim circuit according to Claim 1, wherein said substantially constant feedback path is adapted to reduce instability in said voltage trim circuit.

8. (currently amended) A method of trimming a voltage comprising:

receiving an input voltage to be trimmed;

performing a constant load current and constant feedback impedance voltage trim process on said input voltage; and

outputting a trimmed voltage from said input voltage.

9. (currently amended) The method according to Claim 8, wherein said constant load current and constant feedback impedance voltage trimming process on said input voltage comprises:

selectively adjusting a load resistance wherein a substantially constant load current is maintained;

selectively adjusting a divider ratio wherein a desired output voltage is generated; and

maintaining a substantially constant feedback impedance for each selected load resistance.

10. (original) The method according to Claim 9, wherein said selectively adjusting said load resistance comprises selectively shunting one or more resistors of a bias current circuit.

11. (original) The method according to Claim 9, wherein said selectively adjusting said divider ratio comprises selectively coupling an appropriate one of a plurality of nodes of a voltage divider circuit to an output.

12. (original) The voltage trim circuit according to Claim 9, wherein said maintaining said substantially constant feedback impedance comprises fixedly coupling a particular node of a voltage divider circuit to an input of an operational amplifier.

13. (original) A system of generating a desired output voltage from an input voltage utilizing a voltage trim circuit comprising:

an operational amplifier;

a transistor coupled to said operational amplifier;

a voltage divider coupled to said transistor and said operational amplifier and for selectively adjusting a divider ratio to generate said desired output voltage and for maintaining a substantially constant feedback impedance over a range of input voltage levels; and

a bias current circuit coupled to said voltage divider circuit and for selectively adjusting a resistance to maintain a substantially constant load current over said range of input voltage levels.

14. (original) The system according to Claim 13, wherein said substantially constant load current flows through said transistor.

15. (original) The system according to Claim 13, wherein said substantially constant load current and said substantially constant feedback impedance are adapted to reduce instability in said voltage trim circuit.

16. (original) The system according to Claim 13, wherein said voltage divider circuit comprises:

a first plurality of resistors coupled in series; and

a plurality of selector elements, wherein each selector element is coupled between a corresponding node of said first plurality of resistor coupled in series and an output.

17. (original) The system according to Claim 16, wherein each of said first plurality of resistors have substantially equal resistance.

18. (original) The system according to Claim 13, wherein said bias current circuit comprises:

a second plurality of resistors coupled in series; and

a plurality of shunt elements, wherein each shunt element is coupled in parallel with one of said second plurality of resistors.

19. (original) The system according to Claim 18, wherein said second plurality of resistors comprise:

a first set of binary weighted resistances; and

a second set of binary weighted resistances.

20. (original) The system according to Claim 18 wherein said bias current circuit further comprises an additional resistor coupled in series with said second plurality of resistors.